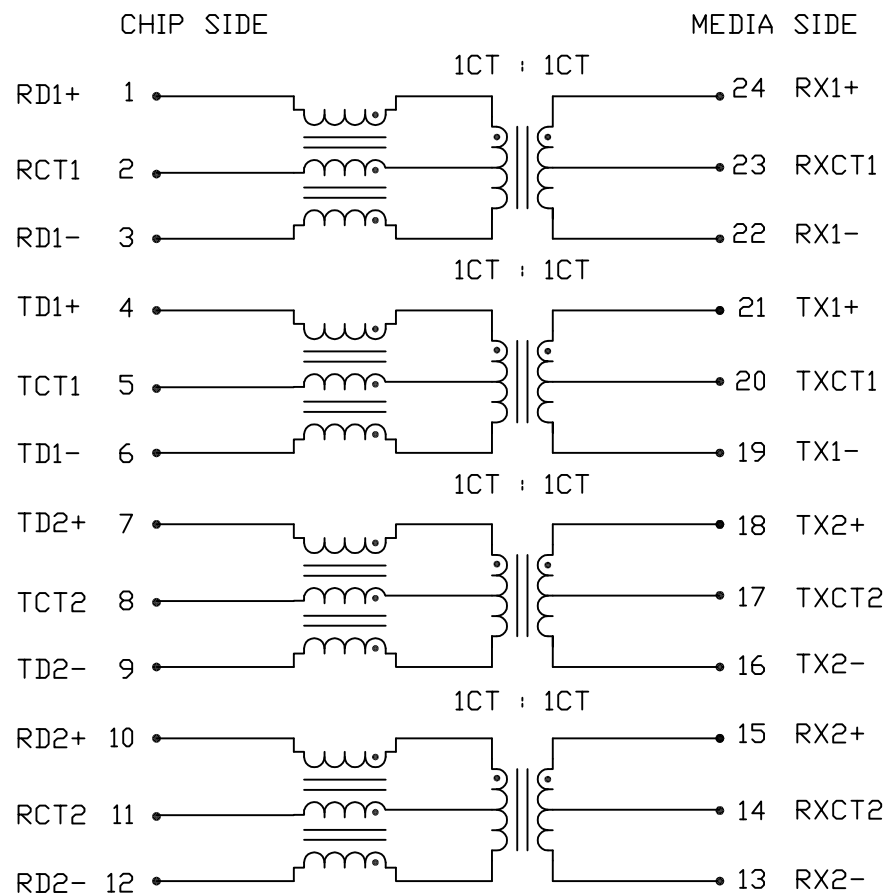


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ELECTRICAL CHARACTERISTICS (@25°C)



SCHEMATIC



URNS RATIO

CHIP SIDE : MEDIA SIDE

1CT : 1CT

POLARITY

PER DOT CONVENTION

□CL

MEDIA SIDE

350μH MIN
@100kHz, 100mVrms
WITH 8mA DC BIAS

INSERTION LOSS

300kHz
1MHz TO 100MHz
125MHz

1.2dB MAX
1.0dB MAX
3.0dB MAX

RETURN LOSS

1MHz TO 30MHz
30MHz TO 80MHz
100MHz

18dB MIN
12-20LOG(F/80MHz) dB MIN
10dB MIN

CROSSTALK

1MHz
10MHz TO 100MHz

55dB MIN
55-24LOG(F/10MHz) dB MIN

DM TO CM REJECTION

2MHz
30MHz TO 200MHz

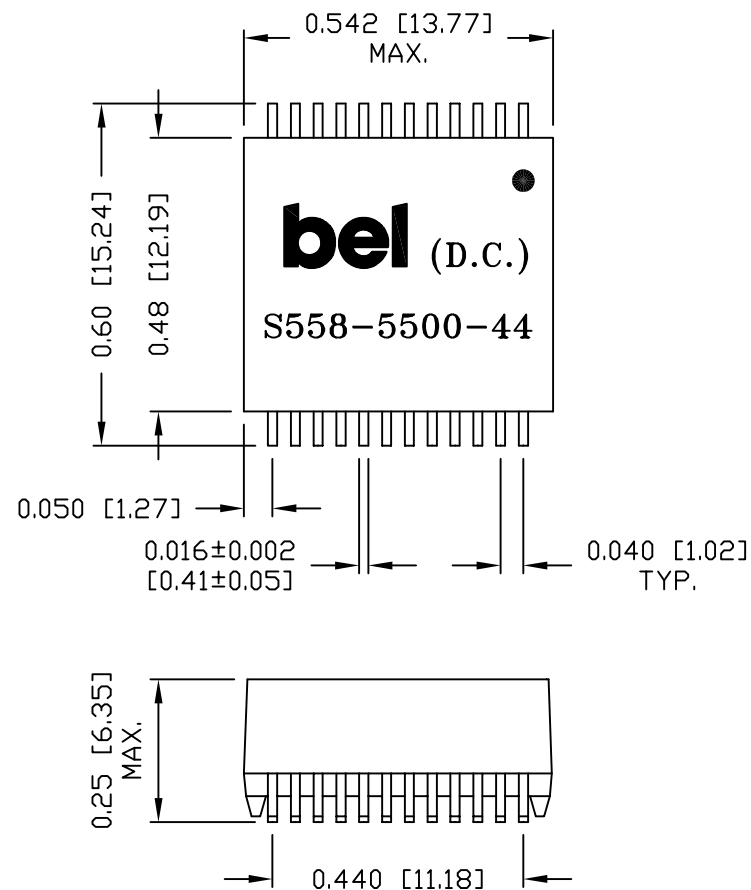
60dB MIN
40-22LOG(F/30MHz) dB MIN

HIPOT : LEAKAGE CURRENT LESS THAN 1mA AT 1500Vrms .

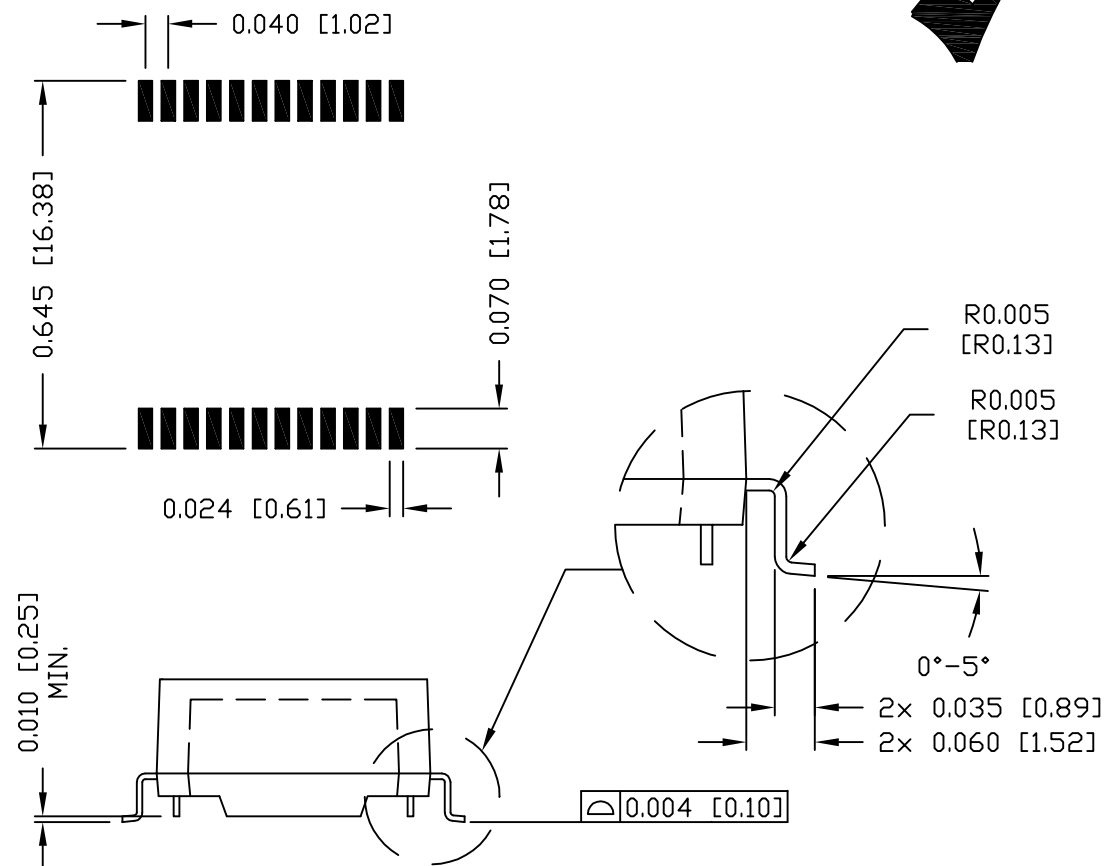
DESIGNED FOR 10/100/1000BT PoE APPLICATIONS, REQUIRING OPERATION
FROM -40 TO 85C, WITH 350mA CURRENT CARRYING CAPACITY.

ORIGINATED BY		DATE	TITLE ELECTRICAL SPECIFICATION S558-5500-44	PART NO. / DRAWING NO.		STANDARD DIM.		[] METRIC DIM. AS REF.		 POWER PROTECT CONNECT
Alice Pang		2021-01-26		S558-5500-44		TOL. IN INCH		UNIT : INCH [mm]		
DRAWN BY		DATE		FILE NAME S558550044A.DWG	.X		SCALE : N/A			
ZC Guo		2021-01-26			.XX		SIZE : A4			
			.XXX							

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SUGGESTED PCB PAD LAYOUT



NOTES:

1. STANDARD MARKING REFER TO DOC. HAND-WORK-04.
2. PACKAGE CODE: "QSS001".

ORIGINATED BY	DATE	TITLE	PART NO. / DRAWING NO.	STANDARD DIM.	[] METRIC DIM. AS REF.	REV. : A	PAGE : 3
Lawrence Tsang	2021-01-26	MECHANICAL OUTLINE S558-5500-44	S558-5500-44	TOL. IN INCH	UNIT : INCH [mm]	 POWER PROTECT CONNECT	
DRAWN BY	DATE		FILE NAME	.X	SCALE : N/A		
ZC Guo	2021-01-26		S558550044A.DWG	.XX ±0.01	SIZE : A4		
				.XXX ±0.005			